

Evolving Verification Capabilities



NOW OFFERING ALL
INSTRUCTION IN A
SINGLE CLASSROOM.

Academy Format

The Verification Academy is organized into a collection of free online courses (modules) and resources, focusing on key aspects of advanced functional verification. Each module consists of multiple sessions—allowing the participant to pick and choose specific topics of interest, as well as revisit any specific topics for future reference. In addition, each session identifies its appropriate target audience, which includes:

Crawl: content is technical, but at an introductory level, and of interest to novice engineers.

Walk: content is of general interest, particularly to managers, but also engineers.

Run: content is technical in nature, and of interest to engineers.

The Verification Academy will provide you with a unique opportunity to develop an understanding of how to mature your organization's processes so that you can then reap the benefits that advanced functional verification offers.

UVM/OVM

The Verification Academy is the most complete UVM/OVM Online resource. You'll find everything you need to get up to speed on UVM and OVM, whether it's downloading the kit(s), the documentation and code examples from the UVM/OVM Online Methodology Cookbook, discussion forums or online training modules.

UVM Express: A collection of techniques, coding styles and UVM usages that are designed to increase the productivity of functional verification. The techniques include raising the abstraction level of tests, writing tests using BFM function and task calls, adding functional coverage, and adding constrained-random stimulus generation.

UVM Connect: A new open-source UVM-based library that provides TLM1 and TLM2 connectivity and object passing between SystemC and SystemVerilog UVM models and components. It also provides a UVM Command API for accessing and controlling UVM simulation from SystemC (or C or C++).

Overview:

- Industry recognized Subject Matter Expert commentary spanning multiple Verification disciplines giving you a broad perspective and knowledge of the subject being covered.
- Thirteen Modules providing you with over twenty hours of instructional material that can be applied immediately in your work environment.
- Global Audience; subtitle captioning in English, Russian, Japanese, Chinese (Simplified & Traditional) allowing dispersed teams to learn together.
- Video content accessible in multiple formats including tablet and mobile devices so you can view on the go.
- The UVM/OVM Online Methodology Cookbook features extensive documentation and code examples that are only available for download on the Verification Academy.

Modules Available:

UVM Express

The UVM Express module introduces UVM Express, discusses how to get organized with test environments, and suggests creating BFM (Bus Functional Models) with tasks in order to facilitate test writing. You will also find a Functional Coverage session that describes how to add functional coverage to an existing BFM based testbench. Constrained-Random Stimulus will also be covered, reviewing how to add constrained-random stimulus generation to an existing BFM based testbench.

Basic UVM (Universal Verification Methodology)

This session gives an overview of UVM, describes the motivation and benefits, and introduces some technical highlights. In addition walks through a short, simple example to get you started with UVM. Also discusses how to connect a UVM testbench to the DUT and how to share information around the testbench using the configuration database. Additional topics include; connecting components, transactions, sequences and tests, monitors and subscribers and lastly, message reporting in UVM, with simple ways in which reporting can be customized.

Basic OVM (Open Verification Methodology)

The goal of the OVM Basics module is to raise your skill level to the point where you have sufficient confidence in your own technical understanding. Thus, giving you the confidence required to start the process of adopting advanced functional verification techniques. This module is primarily aimed at existing VHDL and Verilog engineers or managers who recognize they have a functional verification problem but have little or no experience with constrained-random verification or object-oriented programming.

Advanced OVM & UVM

The goal of the Advanced OVM & UVM modules is to improve your understanding so you can move beyond basic block-level testbenches. Building on the concepts discussed in the basic modules, you will learn how to assemble multi-level environments with layered stimulus sequences to handle more complex verification challenges.

Intelligent Testbench Automation

Over the past few years, the industry's leading functional verification engineering teams have begun turning to a new and emerging technology called Intelligent Testbench Automation ("iTBA"). iTBA combines the high quality of directed testing with the high quantity of constrained random testing, and can be easily integrated into existing verification environments. This module provides a complete introduction to iTBA, showing how you can achieve your coverage goals >10X faster, leaving you the option to reduce your verification time, expand your coverage targets even further, or both.

Verification Planning and Management

The verification of any design of size is a daunting task that requires successful forethought in the form of formulating, architecting, strategizing and documenting an overall verification blueprint. The value of creating such a blueprint at the start of a project has been proven out thru gathered metrics of successful projects.

This verification planning and management (VPM) module is a 3 part, 90 min introduction towards creating such a verification blueprint.

Assertion-Based Verification (ABV)

With the advent of standardized assertion languages and assertion libraries, the industry has recently witnessed an increased interest in adopting assertion-based techniques. This module introduces a set of steps for advancing an organization's ABV skills, infrastructure, and metrics for measuring success while identifying process areas requiring improvement. Simulation-based ABV methods are used throughout the methodology introduced.

FPGA Verification Capabilities

The change in FPGA capabilities has resulted in the emergence of advanced FPGA system-on-chip (SoC) solutions, which includes the integration of third-party IP, DSPs, and multiple microprocessors—all connected through advanced, high-speed bus protocols. Accompanying these changes has been an increase in design and verification complexity, which traditional FPGA flows are generally not prepared to address. This module introduces techniques for addressing complexity by evolving your organization's FPGA verification process capabilities.

Clock-Domain Crossing Verification (CDC)

For the past dozen or so years, static timing analysis has served the industry well by ensuring that all synchronous design blocks will not violate any of the design's setup and hold-timing constraints. This module introduces a set of steps for advancing an organization's clock-domain crossing verification skills, infrastructure, and metrics for measuring success while identifying process areas requiring improvement.

Evolving Verification Capabilities

Ensuring functional correctness on RTL designs continues to pose one of the greatest challenges for today's ASIC, FPGA and SoC design teams. This module provides a common framework for all advanced functional verification modules contained within the Verification Academy. A simple Evolving Capabilities model is presented, which can be used as a tool for assessing an organization's functional verification process capabilities.

Acceleration of SystemVerilog Testbenches with Co-Emulation

This module will give you the confidence required to start the process of investigating and creating a single testbench environment that can be used for both simulation as well as hardware-assisted acceleration. The module is primarily aimed at existing SystemVerilog H/W engineers or managers who recognize they have a functional verification throughput problem but have little or no experience with using emulation as a means for accelerating SystemVerilog testbench environments.

Acceleration of SystemC and TLM 2.0 Testbenches with Co-Emulation

This module advocates that functional verification through modern SystemC testbenches paired with co-emulation enables further verification productivity improvements in terms of raw performance. SystemC simulation combined with co-emulation will deliver dramatic speedup of execution of verification. This module will give you the confidence required to start the process of investigating and creating a single testbench environment that can be used for both simulation as well as hardware-assisted acceleration.

